

Switching Energy and Device Size Limits on Digital Photonic Signal Processing Technologies

Kerry Hinton, Garvesh Raskutti, Peter M. Farrell, Rodney S. Tucker *Fellow IEEE/OSA*

Abstract: The relationship between device size and power consumption of photonic signal processing devices is derived using device specific models for photonic signal processing using semiconductor optical amplifiers, periodically poled lithium niobate and highly non-linear fibres. The results are then compared with the power-length characteristics of CMOS digital devices. The general conclusion is that photonic signal processing technologies demand significantly larger space and/or power than CMOS technologies

Index terms: CMOS, photonic signal processing, power demand

I. INTRODUCTION

Despite advances in electronic technologies, it is expected that the capacity growth of Internet traffic is still so rapid that it will out-pace improvements in the capacity of electronic IP routers. On the other hand, recent generations of dense wavelength division multiplexing (DWDM) optical communications systems have capacities in excess of 1 Tbit/s [1]. This disparity between the data transmission rate of optical systems and the limited switching speed of electronic systems has lead to the term “electronic bottleneck” [2,3]. The apparent disparity between the processing speeds of electronics and photonics has stimulated much research into photonic signal processing technologies [4,5,6] in an attempt to overcome the bottleneck.

Digital signal processing speed is only one of several issues that telecommunications providers consider when deploying new network equipment. For example, due to the ever increasing amount of traffic there is a strong push toward smaller foot-print and more energy efficient equipment in telecommunications networks [7]. This push has arisen from the recognition by service providers that operational cost (OPEX) of powering, maintaining and managing network equipment is a significant contributor to total network system costs [8,9,10].

It has been proposed that photonic technologies can be used to resolve the issues of processing speed, cost, size and energy consumption in the future communications networks [11,12].

Photonic signal processing has been under active investigation for many years. Technologies that have attracted significant interest include the semiconductor optical amplifier (SOA) [13,14,15,16], periodically-poled lithium niobate (PPLN) [17,18,19] and highly non-linear fibre (HNLF) [20,21,22].

A key question, then, is do photonic signal processing technologies have the potential to replace electronics in situations where the electronic bottleneck is a problem? To answer this question it is necessary to evaluate the practicalities of replacing electronic technologies with photonics. Because of the importance of minimizing device footprint and energy consumption it is necessary to consider the footprint and energy consumption of non-linear photonic technologies along with their electronic counterparts.

In this paper we derive relationships between size and power consumption of nonlinear photonic logic devices and compare these photonic devices with electronic devices based on CMOS. The approach uses several device specific models and includes the particular characteristics of devices based upon semiconductor optical amplifiers, periodically-poled lithium niobate and highly non-linear fibres. The results show that photonic signal processing technologies demand significantly larger space and/or power than CMOS technologies.

II. DIGITAL SIGNAL PROCESSING DEVICES AND CIRCUITS

In this section we define some key parameters of digital signal processing devices and circuits. These parameters are used in the following sections as a basis for our analysis of different device technologies. Fig. 1 shows a simple block diagram of a digital signal processing device or circuit. This diagram applies equally to optical, electronic, and optoelectronic signal processing. Typically, the device or circuit will have two or more signal inputs (Fig. 1 shows two inputs) and one or more signal outputs (Fig. 1 shows one output). Also shown in Fig. 1 is a power supply input. The power supply is a key requirement in all devices and circuits. In optical devices the inputs and outputs are optical signals, and in electronic devices they are electrical. In two-input electronic gates Input 1 and Input 2 can generally be treated interchangeably. However, this may not be so for optical devices. Therefore in some circuits considered here, one of the input signals will be labelled as a “control” signal that controls the function of the device or circuit. The signal and control inputs and outputs in Fig. 1 are digital signals. In other words,

ARC Special Research Centre for Ultra-Broadband Information Networks, Department of Electrical and Electronic Engineering, University of Melbourne, Victoria, 3010, Australia.

Email: k.hinton, r.tucker, p.farrell@ee.unimelb.edu.au

This work is supported by the Australian Research Council and Cisco Systems.

they are expected to have only two possible “logic states”, corresponding to logic levels of “1” and “0”.

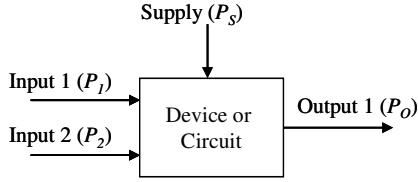


Fig. 1: Digital signal processing device or circuit.

Fig. 2 shows two examples of digital signal processing circuits. Fig. 2(a) is a simplified schematic of a semiconductor optical amplifier (SOA) configured for use as an optical gate or as a wavelength converter using cross-gain modulation [14]. A continuous wave (CW) input signal at wavelength λ_1 (Input 1) is combined with a second input signal carrying data at a different wavelength (λ_2) (Control) and injected into the active region of the SOA. The power supply provides a bias current i_b . (Note that in some optical signal processing circuits, such as logic gates based on highly-nonlinear fibre (HNLF), the power supply is an optical signal.) If the circuit in Fig. 2 (a) is operated with appropriate signal levels, the data on Input 2 causes the gain of the SOA to be modulated, and this data is transferred to the signal at wavelength λ_1 . This wavelength-converted signal at λ_1 appears at the output. Fig. 2(b) is the circuit of a two-input CMOS NAND gate. In this circuit, power to the four CMOS transistors $T_1 - T_4$ is supplied via a voltage supply rail. For the NAND gate in Fig. 2(b), the input and control inputs are interchangeable.

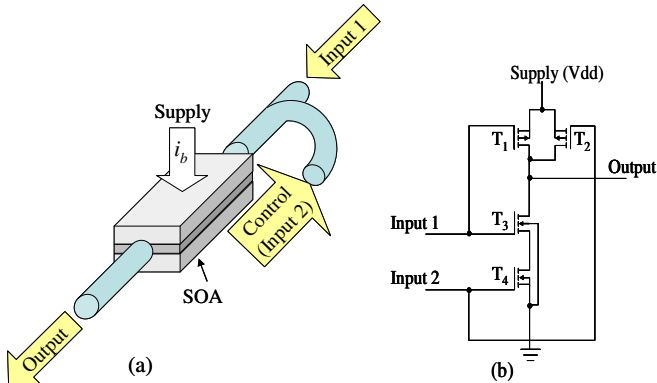


Fig. 2 Examples of digital signal processing circuits. (a) a possible SOA configuration for optical gate, or wavelength converter, with a supply current i_b . (b) CMOS NAND gate. $T_1 - T_4$ are CMOS transistors with supply voltage rail, V_{dd} .

A. Signal levels and Cascadability

To ensure that devices or circuits can be cascaded with other similar devices, or otherwise connected into different circuit arrangements, it is important that the input and output signal levels are compatible. For correct operation, logic circuits must provide (a) cascadability, i.e. the output of one device must be able to drive the input of the next, (b) logic functionality (c) a fan-out capability of at least 2, (d) logic

level restoration, i.e. the outputs have less variation than inputs, input/output, and (e) isolation, i.e. reflections back into the output must not influence the device.

Conditions (a), (c) and (d) above require that a logic device will give the correct output level even if there is a small error in the signal level of an input signal to the device. To illustrate this Fig. 3 shows typical input/output transfer characteristic of a CMOS logic gate [23]. From Fig. 3, we see that the transition between the logical “0” and “1” state for CMOS is abrupt. This transition means multiple devices can be reliably cascaded for CMOS. In particular, it satisfies condition (d) in that small errors in the input signal will still give a correct output level.

In contrast to CMOS the transfer characteristic for PPLN [24], HNLF [20], SOA in a cross gain modulation configuration [25] and SOA in a cross phase modulation configuration [26] devices are typically not as abrupt and are not flat outside the transition between the two logic states. As a consequence the transfer characteristics for these devices do not always satisfy conditions (a) and (d).

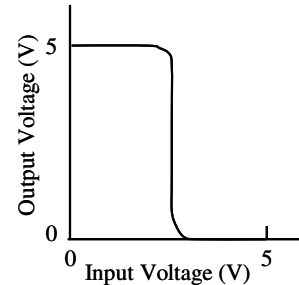


Fig. 3 Input to output signal level transfer characteristic for CMOS logic [23].

As an example, the transfer input/output transfer characteristic for HNLF is shown in Fig. 4 [20]. This device also fails to satisfy condition (a) in that, by itself, its output cannot drive the input of the next device. This is because this device requires an input power of approximately 600 mW to attain a logic “1” output. However, the characteristic shows the corresponding output is only 200 mW, which is insufficient to drive the next device to a logic “1” level. The analysis presented in this paper assumes that gain blocks are provided, if necessary, to ensure that the output signal levels are the same as the input signal levels.

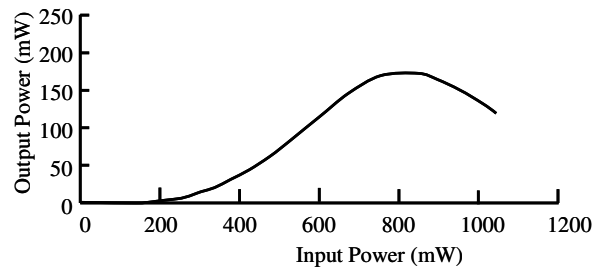


Fig. 4 Control input to output signal transfer characteristic for HNLF, taken from [20].

We also note that the transfer characteristic in Fig. 4 is not flat outside the transition region between the low and high

output states. Therefore, unlike CMOS, variations in the input power will cause variations in the output power. This problem also exists for devices that use CPM, which are typically placed within a Mach Zehnder interferometer configuration (see Fig. 5 for an example), which gives a sinusoidal transfer characteristic [26]. Consequently, accurate control over the input logic levels are required to ensure the interferometer is operating with the required phase delay.

Because optical signal processing circuits generally do not have the abrupt step-like characteristics of CMOS, the quality of a digital optical signal can degrade as it passes through multiple devices. This situation can be exacerbated by spontaneous noise build up. A common way to characterize the quality of an optical signal is the extinction ratio, which is defined as the ratio between these “1” and “0” level signals. Thus the extinction ratio ER is given by

$$ER = \frac{\text{Power Level "1"}}{\text{Power Level "0"}}. \quad (1)$$

In the analysis presented in this paper, we shall require that $ER \geq 10$ for the digital photonic devices to ensure that signal quality is maintained.

B. Power consumption and Switching Energy:

The total power P_T consumed by a device or circuit is the sum of the input power P_1 at Input 1 the input power P_2 at Input 2 and the supply power P_s minus the output signal power, P_o . The total switching energy E_T of the device is given by

$$E_T = P_T \tau_b = (P_1 + P_2 + P_s - P_o) \tau_b \quad (2)$$

where τ_b is the bit period.

For CMOS, this energy per bit is dominated by the energy required to charge the device gate capacitance and the interconnect wires between devices [23]. However, it has become common in the optical literature to define the switching energy of an optical device as the energy required at one input to cause the device to perform a logic operation. In other words, the energy per bit is often defined as $P_1 \tau_b$ or $P_2 \tau_b$. This is not correct because it generally results in a gross underestimation of the energy required to operate the device.

An important difference between the nonlinear photonic devices we consider here and CMOS, is that in CMOS most of the switching energy is consumed during transitions from “0” to “1” and from “1” to “0”. [23] In contrast photonic devices usually continue to consume energy between the transitions. For example, in an SOA wavelength converter or 2R regenerator, the device consumes supply energy continuously. In the SOA gate depicted in Fig. 2 (a), a “low” state at the SOA output is maintained by saturating the SOA gain. This requires a continual supply of high optical power to the control input. Similar requirements hold for PPLN and HNLF.

One of the key motivations for the use of photonic devices in optical signal processing (i.e. signal processing of optical signals) is that the inputs and outputs are in optical form and are compatible with other optical devices. If CMOS is used in optical signal processing it is necessary to convert input signals to electronic form and then back to optical form after processing. This process of O/E/O conversion results in additional power consumption and increases the footprint of the circuit. Therefore, when comparing optical and electronic signal processing circuits, the power consumption and physical size of the O/E/O conversion needs to be considered [27].

III. POWER AND SIZE REQUIREMENTS OF PROCESSING DEVICE TECHNOLOGIES

In this Section we develop detailed power-length relationships for SOA, PPLN and HNLF devices technologies. These models include details such as power supply, phase matching, device efficiency and losses and the device structure. We calculate the energy-length relationship to the nearest order of magnitude since the precise values depend on the particular application and fabrication of the device. The values of constants used in this section are listed in Table 1.

Table 1: Constants used in calculation of power requirements of photonic signal processing technologies.

Symbol	Explanation	Value
w	width of all optical devices	$\sim 10^{-6}$ m
d	thickness of all optical devices	$\sim 10^{-6}$ m
λ	optical wavelength	$\sim 10^{-6}$ m
α_{SOA}	loss coefficient of SOA	$\sim 10^4$ m ⁻¹
q	electron charge	1.6×10^{-19} C
β	linewidth enhancement factor	3 - 5
n_0	carrier density of SOA at transparency	$\sim 10^{24}$ m ⁻³
Γ	SOA confinement factor	~ 0.25
V_b	SOA forward bias voltage	~ 1 V
τ	carrier lifetime of SOA	$\sim 10^{-9}$ s
r_2	Pockels co-efficient of LiNbO ₃	$\sim 10^{-11}$ m/V
n	refractive index of LiNbO ₃	2-4
ϵ_0	permittivity of free-space	8.85×10^{-12} F/m
r_3	Kerr co-efficient for HNLF	$\sim 10^{-18}$ m ² /V ²
α_{HNLF}	loss coefficient of HNLF	~ 1 m ⁻¹

Quantum vacuum noise is the dominant noise source at the operational frequencies of these devices (~ 200 THz) [28]. Very low error rates can be attained in intensity modulated optical systems with photon counts lower than 100 [28], which corresponds to an average signal power, P_1 , of order 10^{-4} Watts (at 100 Gbit/s). In this section we calculate the control, P_2 , and supply, P_s , powers required for photonic technologies. We will find that $P_1 \ll P_2 + P_s$. Therefore, we can ignore the input signal power in our calculations of the device total power requirements.

A. Semiconductor Optical Amplifiers

A digital gate or switch can be implemented using three physical processes in SOA's. These processes are: cross gain modulation (CGM), cross phase modulation (CPM) and four wave mixing (FWM) [15]. All three processes require at least one SOA plus other optical devices such as optical filters, optical gain block (such as another SOA) and Mach Zehnder interferometers. For example CGM and FWM will require optical filtering, to remove unwanted frequencies from the output fibre. The CPM places the SOA in a Mach Zehnder interferometer configuration, as depicted in Fig. 5. In this paper we calculate the total size and power of the active components of the device.

For all three processes the logical state of the control signal is used to determine the logical state of the output for a given input signal logical state. The control signal is coupled into the SOA active region where it interacts with the input signal. Fig. 2 (a) shows one approach for coupling the input and control signals into the SOA. For this to occur, the SOA must be appropriately biased. This is provided by the supply bias current, i_b .

In this Section, we calculate the required control signal power to provide an $ER \geq 10$ for an SOA based gate for each of the three physical processes. We also calculate the power consumed by the device bias supply. From these results, we calculate the total device power consumption.

(i) Cross Gain Modulation (CGM) Control Signal Power

In the CGM configuration, shown in Fig. 2 (a), the supply current, i_b , biases the device to ensure the required level of gain. The control signal power, P_c , is used to move the SOA into and out of gain saturation. This, in turn regulates the output signal level to attain a required extinction ratio between the logical 1 and 0 levels. We now determine the control power, P_c , required for a given extinction ratio, ER , for the CGM configuration. The gain of the SOA can be expressed as [29];

$$G = \exp\left(\frac{g_0 L}{1 + P_c/P_s}\right) = (G_0)^{\frac{1}{1 + P_c/P_s}} \quad (3)$$

where G_0 is the unsaturated end-to-end gain, L is the SOA length, P_s is the SOA gain saturation power and the unsaturated material gain, g_0 , is given by [30]

$$g_0 = \Gamma \alpha_{SOA} \left(\frac{i_b}{i_t} - 1 \right) \quad (4)$$

where Γ is the confinement factor, i_t is the transparency current which corresponds to transparency ($g_0 = 0$) and α_{SOA} is the SOA material loss. The transparency current it is given by

$$i_t = \frac{qwdLN_0}{\tau} \quad (5)$$

where q is the electronic charge, N_0 is the conduction band carrier density required for transparency $\approx 10^{24} \text{ m}^{-3}$, τ is the carrier spontaneous decay lifetime $\approx 10^{-9}$ sec, w is the active region effective width, d is the active region depth and L is the active region length (in metres). The SOA active region width, w , and height, d , are approximately equal to the wavelength of the optical field [15]. Therefore have $w \approx d \approx 10^{-6}$ m. Substituting the values listed in Table 1, into (5) gives

$$i_t (\text{Amps}) \approx 100L (\text{metres}). \quad (6)$$

Using the (3) above, we find the extinction ratio, ER , is dependent upon P_c ;

$$ER = \frac{G_0}{G} = \exp\left(\frac{g_0 LP_c}{P_s + P_c}\right). \quad (7)$$

Therefore, for extinction ratio between 10 and 20 dB with a cross gain modulation SOA based device, we require

$$\frac{g_0 LP_c}{P_s + P_c} \approx 4. \quad (8)$$

(ii) Cross Phase Modulation (CPM) Control Signal Power

We now determine the control power requirements for a cross phase modulation based SOA gate. One way to construct a gate using CPM, is to place the SOA within a Mach Zehnder configuration, as depicted in Fig. 5. The input splitter provides a split ratio of 50/50. The output combiner then re-combines the two separated field components. The phase of the field component which has propagated through the SOA is controlled by P_c . If the phase offset between the two field components at the output is a multiple of 2π , then there is a non-zero output field resulting from constructive interference. If the phase offset is an odd multiple of π , there is no output field due to destructive interference. This will give a very high ER because the logical "0" power level will be close to zero.

The phase delay change, $\Delta\phi$, and saturated gain, G , are related by [31]

$$\Delta\phi = 2\beta \ln(G_0/G) \quad (9)$$

where β is the linewidth enhancement factor ($\beta \approx 3$ to 5 for SOAs). Using (7), for a phase shift of π , this gives

$$\frac{g_0 LP_c}{P_c + P_s} \approx \frac{\pi}{2\beta}. \quad (10)$$

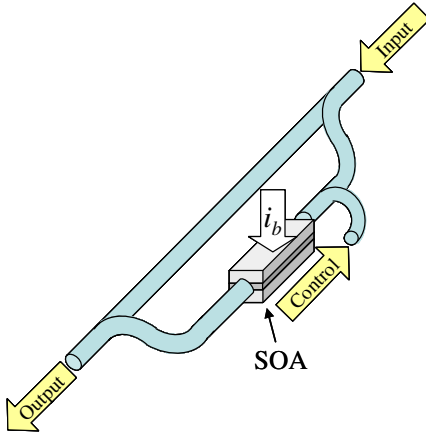


Fig. 5 SOA in Mach Zehnder configuration used for a CGM controlled switch or gate.

(iii) Four Wave Mixing (FWM) Control Signal Power

Signal processing based on FWM requires a high power pump signal in addition to the two input signals and the supply. The extra pump is required to generate a frequency-shifted output signal within the non-linear material of the device. (Four wave mixing involves three input wavelengths to produce the fourth, output, wavelength.) The conversion efficiency, η , of this process is defined as the ratio of the output signal power, P_{out} , to the input control signal power, P_c :

$$\eta = \frac{P_{out}}{P_c}. \quad (11)$$

It has been shown that the pump signal power, P_p , required for maximum efficiency of a SOA gate, based on FWM, dominates the optical input signal powers [32]. That calculation also shows that the maximum efficiency is $\eta \sim 0.1$ and is attained when [32]

$$\frac{g_0 L P_p}{P_p + P_s} \approx 2. \quad (12)$$

(iv) Total SOA Device Power

We now calculate the total power consumption in SOA based gates which including the bias supply power and the optical input power. To do this we note from (8), (10), and (12) that the dominant input optical power, P_d , has the form

$$P_d = \frac{K P_s}{g_0 L - K} \quad (13)$$

where $K \sim 4$ for CGM, $K \sim \pi 2\beta$ for CPM and $K \sim 4$ for FWM.

The bias power contribution is given by, $P_b = V_b i_b$, where V_b is the bias voltage, and i_b the bias current, required to maintain an appropriate carrier concentration. Therefore, using (4), (6)

and (13) the total non-signal power $P_T = P_b + P_d$ can be expressed as

$$P_T = P_b + P_d = i_b V_b + \frac{10^2 K P_s}{\Gamma \alpha_L (i - 10^2 L) - 10^2 K}. \quad (14)$$

From (14), we see that, for a given SOA, the device power is determined by the bias current, i , the device length, L and the constant K . We select a bias current that minimises the P_T . Minimising (14) with respect to i_b gives the SOA device power

$$P_T \approx 100 L V_b + \frac{100 K V_b}{\Gamma \alpha_L} + 10 V_b \sqrt{\frac{K P_s}{\Gamma \alpha_L}} + 10 \sqrt{\frac{K P_s}{\Gamma \alpha_L V_b}}. \quad (15)$$

SOAs used for optical signal processing have lengths ranging between 300 μm and 2 mm [15]. Substituting typical values (see Table 1) into (15) we get:

$$P_T \approx 100 L + 0.4 K + 0.1 \sqrt{K} \text{ Watts} \quad (16)$$

where L is in metres and K depends on the switch configuration. The lowest value of K gives to lowest power consumption and corresponds to CPM.

For all three values of K , we see that for $L \sim 300 \mu\text{m}$, $P \geq 10^{-2}$ Watts $\gg P_{sig}$, which is consistent with our assumption above.

B. Periodically-Poled Lithium Niobate

Signal processing using PPLN is based upon three-wave mixing in which the control signal is used to produce an output which is frequency-shifted from the input signal [18]. Efficient three-wave mixing in Lithium Niobate requires quasi-phase matching which is attained by periodic polling of the waveguide [33]. The conversion efficiency for PPLN, η , is given by (11) with perfect phase matching of the two input signals. Therefore η becomes [34]

$$\eta = \frac{\pi^2 \mu_0^{3/2} \epsilon_0^{1/2} r_2^2 c^2 L_{PPLN}^2 P_c}{2 \lambda^2 w d} \quad (17)$$

where P_c is the control signal pump power for the PPLN device and L_{PPLN} is its length in meters. By controlling P_c , the (frequency-shifted) output signal can be high power, corresponding to a logical "1", or low power, corresponding to a logical "0" level. Typically conversion efficiencies as high as 0.1 can be achieved in real PPLN waveguides [35], therefore P_c is related to length by

$$\eta \approx 10^3 P_c L_{PPLN}^2. \quad (18)$$

This gives

$$P_c \approx \frac{10^{-4}}{L_{PPLN}^2} \text{ Watts}. \quad (19)$$

Because we require the device to provide cascadability (see Section IIA) an amplifier is generally needed to compensate for the low efficiency of the device and to restore the signal levels. One way to do this is to cascade the PPLN device with an SOA gain block with sufficient gain to compensate for the loss, as depicted in Fig. 6. To minimise power consumption of the gain block we operate the SOA so that its gain is unsaturated. A typical length of a SOA, L_{SOA} , is around $500 \mu\text{m}$ [15]. Using (3), (4) and (5) the power required for an SOA with 10-20 dB gain is $P_{SOA} \approx 10^{-1}$ Watts. So the overall power P in terms of total device length, $L=L_{SOA}+L_{PPLN} > 500 \mu\text{m}$, is

$$P_T = P_{SOA} + P_c \approx 10^{-1} + \frac{10^{-4}}{L_{PPLN}^2} \text{ Watts.} \quad (20)$$

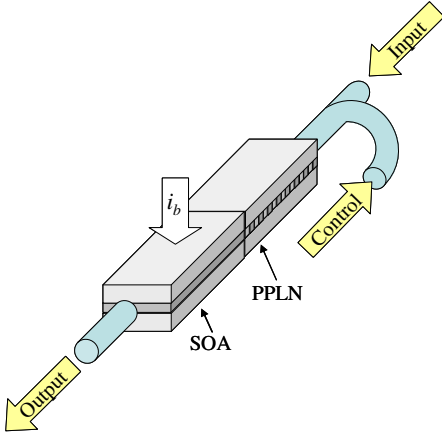


Fig. 6 PPLN based optical gate/switch including the SOA required to compensate for the low conversion efficiency of the PPLN based device.

We see from (20) that the power consumption of the PPLN device can be reduced by increasing L_{PPLN} . However, due to the low efficiency of the PPLN device, there must always be a gain block present. The power consumption of this SOA gain block represents a lower limit on the power consumption of a PPLN based gate. This power is significantly greater than the assumed input signal power $P_{sig} \sim 10^{-4}$ Watts.

C. Highly Non-Linear Fibre (HNLf)

HNLf exhibits a higher Kerr effect coefficient relative to traditional silica optical fibres. There are two phenomena that can be used for signal processing in HNLf. These are: cross-phase modulation (CPM) and four-wave mixing (FWM). We now consider each of these.

(i) Cross-phase modulation

Using CPM the HNLf is placed in one arm of a Mach Zehnder interferometer as depicted in Fig. 7. The control signal with power level P_c is used to control the phase difference between the two arms of the device. Including the impact of the loss, a phase difference of π in a HNLf, requires [36]

$$P_c = \frac{A\lambda}{2L_{eff}r_3} \quad (21)$$

where A is the cross-sectional area of the HNLf, λ is the wavelength of the signal, r_3 is the Kerr co-efficient for the HNLf and L_{eff} is the effective length of the fibre. The effective length is given by [37];

$$L_{eff} = \int_0^L e^{-\alpha_{HNLf}z} dz = \frac{1 - e^{-\alpha_{HNLf}L}}{\alpha_{HNLf}} \quad (22)$$

where L_{HNLf} is the length of the HNLf used in the gate.

Using typical values for α_{HNLf} (see Table 1), gives the relationship between device power and length as;

$$P_T \approx \begin{cases} \frac{1}{L} \text{ Watts,} & L < 1\text{m} \\ 1 \text{ Watt,} & L > 1\text{m} \end{cases} \quad (23)$$

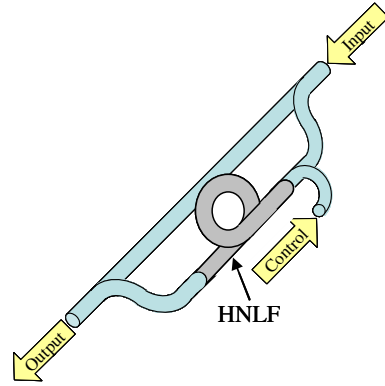


Fig. 7 HNLf based Mach Zehnder optical gate/switch.

(ii) Four-wave mixing

As with PPLN, FWM in HNLf also uses wavelength translation to implement signal processing. For HNLf, the conversion efficiency for FWM, η , is given by [38]

$$\eta = \left(\frac{2\pi r_3}{\lambda w d} P_c L_{eff} \right)^2 \quad (24)$$

where P_c is the control signal power into the fibre and L_{HNLf} its length in meters. Conversion efficiencies, η , up to 0.1 have been achieved in silicon waveguides [38]. Using $\eta = 0.1$, gives

$$P_{HNLf} \approx \frac{10^{-3}}{L_{eff}} \text{ Watts.} \quad (25)$$

With $\eta = 0.1$, as with the PPLN device above, it may be necessary to use a SOA, as depicted in Fig. 8. We again set

Switching Energy, Hinton et al.

$L_{SOA} = 500 \mu\text{m}$. Therefore the total power-length relationship for HLNLF device based upon CPM, is

$$P_T = P_{SOA} + P_{HNLf} \sim 10^{-1} + \frac{10^{-3}}{L_{eff}} \text{ Watts.} \quad (26)$$

The total length of the device is $L = L_{SOA} + L_{eff} > 500 \mu\text{m}$.

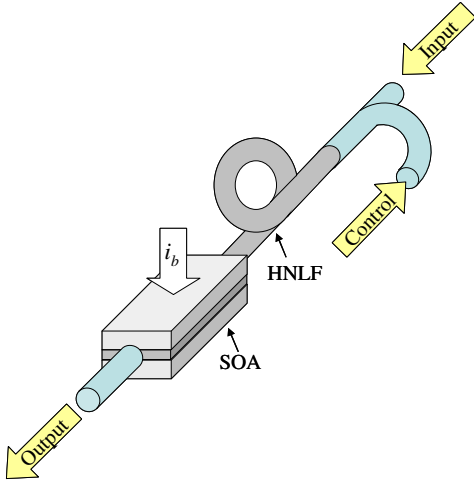


Fig. 8 HNLf optical gate/switch based upon FWM. The SOA is required to compensate for the low FWM efficiency.

IV. DISCUSSION

Fig. 9 shows the energy per bit against the device length for each of these signal processing technologies considered here. In Fig. 9, the operating bit rate is taken as 100 Gbit/s. The data in Fig. 9 is based upon the relationships (16), (20), (23) and (26) as well as (2) to convert the switching power to energy per bit.

Also included in Fig. 9 is the corresponding relationship for CMOS based on the 2005 International Roadmap for Semiconductors [39]. Currently, the average feature size of CMOS devices is approximately 100 nm and the devices consume approximately 0.1 fJ energy per bit [39]. It is predicted that this will be reduced to 10 nm and 0.01 fJ/bit in the coming 10-15 years [39]. The energy consumption scales with the length of the device so as smaller devices are implemented, the energy consumption will also reduce.

When used in an optical communications network CMOS processing in a node or router will require optical/electronic/optical (O/E/O) conversion of the incoming optical data stream. With modern technology, the size of O/E and E/O converters is around 10^{-4}m [40]. Also, we have assumed the O/E/O power consumption is similar to an SOA because the E/O transmitter laser driver will dominate the power consumption. Therefore Fig. 9 includes a shaded region representing the average energy/bit and length for circuits that contain both CMOS devices and O/E/O converters.

The lower left end of the shaded region corresponds to circuits with many CMOS devices per O/E/O converter. In this

case the average length and power consumption including both CMOS devices and O/E/O will be dominated by the CMOS devices. On the other hand, the upper right of the shaded region corresponds to the situation where there are only a few CMOS devices per O/E/O conversion. In this case the average length and power will be dominated by the O/E/O converters.

Fig. 9, shows that the energy per bit in CMOS is less than photonic devices. If we include the power consumption and size of O/E/O conversion with CMOS devices, photonic technologies have power and space requirements similar to CMOS only when the number signal processing devices is small (i.e close to unity). When a significant number of signal processing devices are required, CMOS plus O/E/O has the lowest power/size requirement. This result has been confirmed elsewhere [27].

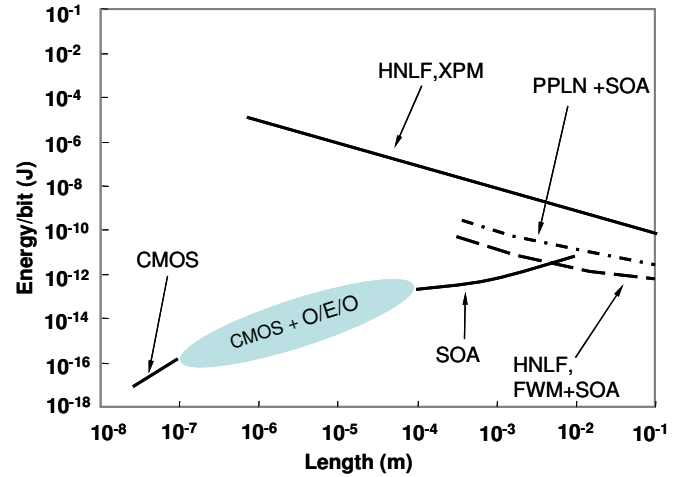


Fig. 9 Energy per bit versus device length for photonic signal processing technologies operating at 100 Gbit/s. Also included is the plot for CMOS and the region for CMOS plus O/E/O conversion.

The results presented in Fig. 9 indicate that only very simple signal processing, such as wavelength conversion and regeneration, are amenable to photonic implementation. CMOS technology is by far the best option for minimising the power consumption and footprint for equipment which undertakes complex processes such as address or label lookup, SDH/SONET frame processing, Forward Error Correction and the like.

V. CONCLUSION

In this paper we have shown that photonic gates based upon SOAs, PPLN and HNLf technologies require significantly greater energy and size than CMOS technology. Further, for some technologies we require precise control of the input power levels as well as extra power to provide an appropriate bias and/or a gain block to ensure the output signal levels are similar to those of the input. With CMOS technologies, these problems do not arise.

The issue of power consumption is already important to network operators and its importance will increase as the

capacity and power demands of the Internet grow with its ubiquity. The results presented in this paper indicate that, due to their high power and space demands, photonic technologies are not well suited for network elements in which processing of the incoming signal requires a large number of devices. However, photonic technologies may be well suited for processes such as all-optical wavelength conversion and signal regeneration, where the number of signal processing devices is small.

Both electronics and optics/photronics present a “bottleneck” of some form which network and systems designers must address. Optimising network performance metrics such as throughput, power consumption, equipment footprint as well as environmental and financial cost, will require the judicious of both technologies.

REFERENCES

- [1] R. Nagarajan, et al. “Single-chip 40-channel IP transmitter photonic integrated circuit capable of aggregate data rate of 1.6Tbit/s”, *Electron Lett.* vol. 42, pp.771-773, 2006
- [2] P. Byvel, “Future high-capacity optical telecommunications networks” *Phil. Trans. R. Soc. Lond. A*, Vol. 358, pp.303-329, 2000
- [3] A. Koonen, I. Monroy, J. Olmos, H. de Waardt, G-D Khoe, “The expected impact of new technologies in communications networks”, *Proc. European Conf. on Networks and Optical Communications*, pp. 1-8, 2003
- [4] Y Ben-Ezra, U. Mahlab, M. Haridim, B. Lembrikov, “Applications of All-Optical Signal Processing in Modern Optical Communications”, *ICTON’07*, pp. 328-331, 2007
- [5] E. Kehayas, et al. “All-Optical Network Subsystems Using Integrated SOA-Based Optical Gates and Flip-Flops for Label-Swapped Networks” *IEEE Photon Technol Lett.*, vol. 18, No. 16, pp. 1750-1752, 2006
- [6] X. Yang, et al. “High-speed All-optical Signal Processing using Semiconductor Optical Amplifiers”, *ICTON’06*, pp. 161-164, 2006
- [7] For example: http://www.nortel.com/products/01/optera/long_haul/dwdm/collateral/n103700-031003.pdf
- [8] O. Gerstel, H. Raza, “Predeployment of Resources in Agile Photonic Networks”, *Jour. Lightwave Technol.* Vol.22, No.10, pp.2236-2244, 2004
- [9] C. Coltra, P. Gabla, P. Gong, M. Cheng, V. Heuer, “Building minimum total cost of ownership optical networks in the Asia Pacific Region”, *Alcatel Telecommunications Review*, 1st Quarter, p.1, 2003
- [10] J. Koomey, et al. “Network electricity use associated with wireless personal digital assistants” *ASCE J. Infrastructure Systems*, vol. 10, pp. 131-137, 2004
- [11] S. Ben Yoo, H. Yang, “Petabit-per-Second Routers: Case for All-Optical over Electronic Implementation”, *OFC’07*, Paper OThF3, 2007
- [12] B. Eggleton, et al. “Chalcogenide glass waveguides and grating devices for all-optical signal conditioning” *OFC’07 Paper OTHP4*, 2007
- [13] T. Houbavlis, et al., “All-Optical Signal Processing and Applications within the Esprit Project DO_ALL”, *J. Lightwave Technol.*, vol.23, pp.781-801, 2005
- [14] K. Stubkjaer, “Semiconductor Optical Amplifier-Based All-Optical Gates for High-Speed Optical Processing”, *IEEE Jour. Selected Topics in Quantum Electron.* Vol.6, No.6, pp.1428-1435, 2000
- [15] C. Schubert et al. “High-speed optical processing using semiconductor amplifiers”, *Jour. Optical and Fiber Comm. Reports*, Vol.2, pp.171-208, 2004
- [16] K. Vlachos, N. Pleros, C. Binitjiax, G. Theophilopoulos, H. Avramopoulos, “Ultrafast Time-Domain Technology and Its Application in All-Optical Signal Processing”, *Jour. Lightwave Technol.* Vol.21, No.9, pp.1857-1868, 2003
- [17] Y. L. Lee, et al., “All-optical AND and NAND gates based upon cascaded second-order nonlinear processes in a Ti-diffused periodically poled LiNbO₃ waveguide”, *Optics Express*, vol.14, pp.2776-2782, 2006
- [18] C. Langrock, S. Kumar, J. McGeehan, A. Willner, M. Fejer, “All-Optical Signal Processing Using $\chi^{(2)}$ Nonlinearities in Guided-Wave Devices”, *J. Lightwave Technol.*, vol.24, pp.2579-2592, 2006
- [19] G. Kanter, P. Kumar, K. Paramesaran, M. Fejer, “Wavelength-Selective Pulsed All-Optical Switching Based on Cascaded Second-Order Nonlinearity in a Periodically Poled Lithium-Niobate Waveguide”, *IEEE Photon. Technol. Lett.*, vol.13, pp.341-343, 2001
- [20] M. Rochette, L. Fu, D. Moss, B. Eggleton, “2R Optical Regeneration: An All-Optical Solution for BER Improvement”, *IEEE J. Sel. Topics Quantum Electron.*, vol.12, pp.736-744, 2006
- [21] M. Asobe, T. Ohara, I. Yokohama, T. Kaino, “Low power all-optical switching in a nonlinear optical loop mirror using chalcogenide glass fibre”, *Electron. Lett.*, vol.32, pp.1396-1397, 1996
- [22] M Asobe, T. Kanamori, K. Kubodera, “Ultrafast All-Optical Switching Using Highly Nonlinear Chalcogenide Glass Fibre”, *IEEE Photon. Technol. Lett.*, vol.4, pp.362-365, 1992
- [23] “CMOS, the Ideal Logic Family”, *Fairchild Application Note 77*, January, 1983
- [24] K. Parameswaran, et al. “Low-power all-optical gate based upon sum frequency mixing in APE waveguides in PPLN”, *IEEE Photon Technol Lett*, vol. 12, pp. 654-656, 2000
- [25] H. Ju, S. Zhang, D. Lenstra, H. de Waardt, E. Tangdiongga, G. Khoe, H. Dorren, “SOA-based all-optical switch with sub-picosecond full recovery”, *Optics Express*, vol.13, pp.942-947, 2005
- [26] G. Gavioli, et al. “Cascadability Properties of Optical #R Regenerators Based on SOAs”. *Jour. Lightwave Technol*, vol. 25, No. 8, pp.2766-2775, 2007
- [27] R. Tucker, K. Hinton, G. Raskutti, “Energy Consumption Limits in High Speed Optical and Electronic Signal Processing” *Electron. Letts*, vol. 43, pp. 906-908, 2007
- [28] D. Marcuse, “Principles of Quantum Electronics”, *Academic Press*, 1980
- [29] I. Maio, “Gain Saturation in Travelling-Wave Ridge Waveguide Semiconductor Laser Amplifiers”, *IEEE Photon. Technol. Lett*, Vol.3, pp.629-631, 1991
- [30] Bahaa E. A. Saleh and Malvin C. Teich, *Fundamentals of Photonics*, John Wiley & Sims, 1991.
- [31] C. Henry, “Theory of the linewidth of semiconductor lasers” *IEEE Jour. Quantum Electron*, Vol.18, pp.259-264, 1982
- [32] A. Mecozzi, “Analytical theory of four-wave mixing in semiconductor amplifiers” *Optics Lett.*, Vol.19, No.12, pp.892-894, 1994
- [33] M. L. Bortz et al., “Noncritical Quasi-Phase-Matched Second Harmonic Generation in an Annealed Proton-Exchanged LiNbO₃ Waveguide” *IEEE J. Quantum Electron.*, vol.30, pp.2953-2960, Dec. 1994.
- [34] L. E. Myers et al., “Periodically Poled Lithium Niobate and Quasi-Phase-Matched Optical Parametric Oscillators” *IEEE J. Quantum Electron.*, vol.33, pp.1663-1672, Oct. 1997.
- [35] Y. L. Lee, et al., “All-optical wavelength conversion and tuning by the cascaded sum- and difference frequency generation (cSFG/DFG) in a temperature gradient controlled Ti:PPLN channel waveguide,” *Optics Express*, vol.13, pp.2989-2993, 2005.
- [36] S.Watanabe, “Optical signal processing using nonlinear fibers”, *J. Optical and Fiber Comms.*, Rep. vol.3, pp.1-24, 2005.
- [37] R. Ramaswami, K. Sivarajan, “Optical Networks: A Practical Perspective”, *Morgan Kaufman*,
- [38] O. Boyraz et al., “All optical switching and continuum generation in silicon waveguides”, *Optics Express*, vol.12, pp.4094-4102, Aug. 2004.
- [39] “International Technology Roadmap for Semiconductors”, 2005 Edition, Executive Summary, International Roadmap Committee, <http://public.itrs.net/>
- [40] R. Nagarajan, et al. “Large-scale photonic integrated circuits for long-haul transmission and switching” *J. Optical Networking*, vol.6, No.2, pp.102-111, 2007

Switching Energy, Hinton et al.

Kerry Hinton received an Honours Bachelor of Engineering in 1978, an Honours Bachelor of Science in 1980 and Master of Science Degree in Mathematical Sciences in 1982, all from the University of Adelaide. He was awarded a Ph.D. in Theoretical Physics from the University of Newcastle Upon Tyne, U.K., in 1984. In that year Dr. Hinton joined Telstra Research Laboratories, Victoria, Australia, and worked on analytical and numerical modelling of optical systems and components. Upon closure of the Telstra Research Laboratories in 2006, Dr. Hinton joined the ARC Special Research Centre for Ultra-Broadband Information Networks, Australia, at the University of Melbourne, Australia, where he has continued his research into optical system technologies and networks.

Garvesh Raskutti received his Bachelor of Science and Bachelor of Engineering degrees from University of Melbourne in 2006. He is currently undertaking a Master of Engineering Science in the Department of Electrical Engineering also at the University of Melbourne on the topic of energy consumption of optical processing devices.

Peter F. Farrell received the Ph.D. degree in atomic physics and laser spectroscopy from Griffith University, Brisbane, Qld., Australia, in 1992. His interest in optical fibre communications systems stems from his postdoctoral employment with Telstra Research Laboratories, Clayton, Vic., Australia, where he worked on erbium-doped fibre amplifiers. He was an Optical Group Leader with Altamar Networks and an Associate Professor with Victoria University, Melbourne, Vic. He is currently an Associate Professor with the Department of Electrical and Electronic Engineering, University of Melbourne, Parkville, Vic.

Rodney S Tucker (S'72-M'75-SM'85-F'90) received the B.E. and Ph.D. degrees from the University of Melbourne, Parkville, Australia, in 1969 and 1975, respectively.

He is a Laureate Professor at the University of Melbourne. He is also the Research Director of the Australian Research Council Special Research Centre for Ultra-Broadband Information Networks (CUBIN), in the Department of Electrical and Electronic Engineering, University of Melbourne. He has held positions with University of Queensland, University of California, Berkeley, Cornell University, Plessey Research, AT&T Bell Laboratories, Hewlett Packard Laboratories and Agilent Technologies.

Prof. Tucker is a Fellow of the Australian Academy of Science and a Fellow of the Australian Academy of Technological Sciences and Engineering. In 1997, he was awarded the Australia Prize for his contributions to telecommunications and in 2007 he was awarded the IEEE LEOS Aron Kressel Award.